UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/653,156	08/31/2000	Vishnu K. Agarwal	MI22-1518	4650

21567 7590 02/21/2006

WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/653,156	AGARWAL ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/1/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 27-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-15 and 28-37* is/are allowed.

6)☒ Claim(s) *1-9 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-15, 27-37 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 4-7, 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Schugraf et al. (U.S. Patent No. 5,885,882).

Referring to figures 3-5, Schugraf et al. teaches a method of fabricating a capacitor comprising:

Forming undoped, rugged polysilicon (20b) over a substrate (10);

Forming first capacitor electrode comprising TiN (30, col. 4, line 33) over the rugged polysilicon, the first electrode (30) having an innermost surface area per unit area and an

outermost surface area per unit area that are both greater than an outer most surface area per unit area of the substrate, the innermost surface of the first electrode comprising a surface of the first electrode that is firstly formed over the substrate(10), and the outermost surface of the first electrode comprising a surface of the first electrode (30) that is lastly formed over the substrate (10) (HSG has a larger surface area than the plain smooth substrate surface, see figures 3-5, col. 3-4);

Schugraf et al. teaches forming a DRAM capacitor. It is inherent that the DRAM capacitor includes forming a first capacitor electrode (30) a rugged polysilicon (20b), and a capacitor dielectric and forming a second capacitor electrode over the dielectric layer.

Regarding to claim 2, the first electrode consists of TiN (see col. 4, lines 55).

Regarding to claim 4, the first electrode (30) is on and in contact with the rugged polysilicon (20b, see figure 5).

Regarding to claim 5, the rugged polysilicon comprises hemispherical grain polysilicon (see col. 4, lines 18-33, noted that annealing would form grain).

Regarding to claim 6, forming the rugged polysilicon comprises using a seed density sufficiently small to yield at least some spaced apart grains (see col. 4, lines 18-33)

Regarding to claim 7, the outermost surface area of the first electrode (30) is at least 30% greater than the outer surface of the substrate (10) (note that the out surface of the substrate is flat, therefore, the outermost surface area of the first electrode is greater than the outer surface of the substrate).

Regarding to claim 27, the TiN (30) forms a continuous layer within the first electrode (see figure 5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3, 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schugraf et al. (U.S. Patent No. 5,885,882) as applied to claims 1-2, 4-7, 27 above in view of Sneh et al. (U.S. Patent No. 6,551,399) and Raaijmakers et al. (U.S. Patent No. 6.780,704).

Referring to figures 3-5, Schugraf et al. teaches a method of fabricating a capacitor comprising:

Forming undoped, rugged polysilicon (20b) over a substrate (10);

Forming first capacitor electrode comprising TiN (30, col. 4, line 33) over the rugged polysilicon, the first electrode (30) having an innermost surface area per unit area and an outermost surface area per unit area that are both greater than an outer most surface area per unit area of the substrate, the innermost surface of the first electrode comprising a surface of the first electrode that is firstly formed over the substrate(10), and the outermost surface of the first electrode comprising a surface of the first electrode (30) that is lastly formed over the substrate (10) (HSG has a larger surface area than the plain smooth substrate surface, see figures 3-5, col. 3-4);

Schugraf et al. teaches forming a DRAM capacitor. It is inherent that the DRAM capacitor includes forming a first capacitor electrode (30) a rugged polysilicon (20b), and a capacitor dielectric and forming a second capacitor electrode over the dielectric layer.

However, the reference does not teach forming the first electrode layer comprising chemisorbing a layer of a first precursor at least one monolayer thick over the substrate; chemisorbing a layer of a second precursor at least one monolayer thick on the first precursor layer, a chemisorption product of the first and second precursor layers being comprising by the first capacitor electrode, the dielectric layer comprises Ta2O5, ZrO2, WO3, Al2O3, HfO2, BST, strontium titanate, and the substrate comprises a bulk semiconductive wafer.

Referring to figures 1-4, Sneh et al. teaches a layer by using ALD technique of a first precursor at least one monolayer thick over a substrate (see col. 4, lines 20+);

Forming a layer by using ALD technique of a second precursor at least one monolayer thick on the first precursor layer (see col. 4, lines 20+), a chemisorption product of the first and second precursor layers being comprised by a first capacitor electrode comprising TiN (11) over the substrate.

Raaijmaker et al. teaches forming a layer by using ALD is called chemisorbing a layer (see col. 7, lines 2-32). Regarding to claim 3, wherein the substrate comprises a bulk semiconductor wafer (called semiconductor substrate (12, see abstract)). Regarding to claim 9, the dielectric layer comprises Ta2O5, ZrO2, WO3, Al2O3, HfO2, BST, strontium titanate (see col. 25, lines 24-44).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form a chemisorbing layer of at least one monolayer

thick in process of Schugraf et al. as taught by Sneh et al. in view of Raaijmaker et al. because the process would provide excellent step coverage and forming a dielectric layer with a high dielectric constant.

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize density of the polysilicon layer and the surface area of the electrode, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.-hydrogenated dielectric layer), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- density of the polysilicon layer and the surface area of the electrode) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form density of the polysilicon layer and the surface area of the electrode in process of Schugraf et al. because discovering the optimum or workable ranges involves only routine skill in the art.

Allowable Subject Matter

Claims 10-15, 28-37 are allowed.

None of the prior art alone or in combination teaches or suggests the particular subset of the process steps in forming an undoped polysilicon over the side and bottom of the opening, and

removing the polysilicon layer from over the bottom of the opening and converting at least some of the polysilicon layer to undoped hemispherical grain polysilicon, forming a first capacitor electrode wherein the outer surface of the first electrode is greater than the outer surface of the substrat, forming a capacitor dielectric layer over the HSG polysilicon, and forming a second capacitor electrode over the HSG polysilicon.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN